Attorney's Docket No. 042390P10625 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In Re Application of:	
Jack Hwang, et al.	Examiner: Igwe U. Anya
Application No.: 09/887,910	Art Unit: 2825
Filed: June 22, 2001	
For: A METHOD OF MAKING A SEMICONDUCTOR TRANSISTOR BY IMPLANTING IONS INTO A GATE DIELECTRIC LAYER THEREOF	

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

APPEAL BRIEF IN SUPPORT OF APPELLANTS' APPEAL TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Dear Sir:

The Appellants hereby submit this Brief in triplicate in support of their appeal from a final decision by the Examiner, mailed November 5, 2003, in the above-captioned case. The Appellants respectfully request consideration of this appeal by the Board of Patent Appeals and Interferences for allowance of the above-captioned patent application.

FIRST CLASS CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on 1-12-04
Date of Deposit

Valerie J. Sterling
Name of Person Mailing Correspondence

Valerie J. Sterling
Signature

1-12-04
Date

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I. REAL PARTY IN INTEREST

The real party in interest is Intel Corporation, a corporation of Delaware having a principle place of business at 2200 Mission College Blvd., Santa Clara, CA 95052.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

III. STATUS OF THE CLAIMS

Claims 1-22 are currently pending. Claims 1-22 currently stand rejected by the Examiner under the Final Rejection mailed August 20, 2003. Claims 1-12, 14, 15 and 20-22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Goeckner et al., US Patent Number 6,335,536 (hereinafter Goeckner) in view of Aronowitz et al., US Patent Number 6,087,229 (hereinafter Aronowitz). Claims 13 and 16-19 stand rejected as being unpatentable over Goeckner in view of Aronowitz and further in view of Chen, US Patent Number 6,432,780 (hereinafter Chen).

IV. STATUS OF AMENDMENTS

A copy of all claims on appeal is attached in Appendix A hereto.

V. SUMMARY OF THE INVENTION

The present invention describes and claims a method of making a semiconductor transistor. A wafer substrate is inserted through the slit into the

chamber and located on the upper surface of a stand. The wafer substrate is at substantially the same voltage as the stand. (Page 9, lines 5-7)

Nitrogen gas is introduced through an inlet port into the chamber and flows into a cylindrical cathode. A constant flow of nitrogen gas flows into the inlet port and out of the outlet port. (Page 9, lines 8-10)

When a voltage is created on the cylindrical cathode, a voltage difference between the cylindrical cathode and the chamber increases. The increase in the voltage difference generates a transient ion plasma out of some of the nitrogen gas. The ion plasma consists of nitrogen ions having positive charge. The plasma is located within the cylindrical cathode above the substrate. An upper edge of the plasma is located near an upper wall of the chamber. A lower edge of the plasma is located distant from an upper surface of the wafer substrate so that a gap exists between the lower edge of the plasma and an upper surface of the wafer substrate. The gap is a few millimeters wide. (Page 9, lines 11-20)

The wafer substrate is made of a doped semiconductor material such as P-doped silicon. A thin gate dielectric layer is formed on the wafer substrate prior to its insertion into the chamber. The gate dielectric layer forms part of a transistor which is subsequently manufactured in and on the wafer substrate. For optimal performance of the transistor, it is required that the gate dielectric layer be very thin and be made of a material with a high k-value. The gate dielectric layer, when inserted into the chamber, is typically made of silicon dioxide having a thickness of approximately 20Å. The silicon dioxide gate dielectric layer is formed by exposing the silicon wafer substrate to oxygen in water. (Page 9, line 21 to Page 10, line 9)

A disadvantage of a silicon dioxide gate dielectric layer is that it has a relatively low k-value of about 3.9. A silicon nitride gate dielectric layer by contrast has a relatively high k-value of about 7.5, which is more desirable. The k-value of a silicon dioxide gate dielectric layer can be increased by implanting nitrogen molecules into the silicon dioxide gate dielectric layer. (Page 10, lines 10-14)

An ion plasma concentration increases when a voltage is applied to the circular cathode. The voltage on the cathode 38 is switched off before the plasma can reach a steady-state condition. The plasma, when existing, is thus in a transient condition at all times. By maintaining the plasma in a transient state the ion energy can be controlled. (Page 10, lines 15-20)

By pulsing the voltage on the stand, a voltage differential of -10 V is created between the stand and the plasma. The voltage potential only exists when an implanting switch is closed. Ions of the plasma are accelerated from the plasma towards the silicon dioxide gate dielectric layer when the implanting switch is closed. When an implanting switch is open, the ions are not accelerated towards the gate dielectric layer. (Page 10, line 21 to Page 11, line 6)

The combined effect of the creation of the confined transient plasma utilizing the plasma generating apparatus and creating a pulsed voltage on the stand, results in tight control in the amount and the energy of ions being implanted into the gate dielectric layer. The energy of the ions being implanted can be sharply defined and controlled for an optimum profile. (Page 11, lines 7-11)

A result of the implantation is that a k-value of the gate dielectric layer is increased while the composition of the silicon of the wafer substrate directly below the silicon dioxide layer remains unchanged. (Page 11, lines 16-19)

The wafer substrate is subsequently removed from the chamber and a multitude of semiconductor devices, including transistors, are formed thereon. A conductive gate is formed directly on the gate dielectric layer. N-doped source and drain regions are formed on opposing sides of the gate. Subsequent metalization and dielectric layers are formed above the transistor. A supply voltage can be provided through one metal line to the source and a drain voltage can be connected to a metal line connected to the drain. When a voltage is applied to the gate, current flows from the source to the drain. The current from the source to the drain is thus switched by applying a voltage to the gate. A switch speed of the current is increased because the gate dielectric layer is relatively thin and its k-value is relatively high. The current from the source to the drain is however not affected by any impurities. (Page 12, lines 3-16)

VI. ISSUES

The issues presented in this appeal are whether claims 1-20 are unpatentable under:

- 35 U.S.C. § 103 as being obvious over Goeckner in view of Aronowitz;

  and

- U.S.C. § 103 as being obvious over Goeckner in view of Aronowitz and further in view of Chen.

VII. GROUPING OF CLAIMS

For the purpose of this appeal, all the claims stand or fall together.

VIII. ARGUMENT; REJECTION OF THE PRESENT INVENTION IS IMPROPER SINCE ONE SKILLED IN THE ART WITH KNOWLEDGE OF THE PRIOR ART WOULD NOT HAVE USED THE PRIOR ART TO COME UP WITH THE INVENTION AS CLAIMED

Claim 1 recites:

> 1. A method of making a semiconductor transistor, comprising:
> locating a substrate of a doped semiconductor material in a chamber;
> introducing a gas into the chamber;
> repeatedly increasing and decreasing a plasma generating voltage potential across the gas in the chamber between a cathode and an anode while the substrate is in the chamber, a transient ion plasma generating from the gas after an increase in magnitude of the plasma generating voltage potential and degenerating after a decrease in magnitude of the plasma generating voltage potential;
> repeatedly increasing and decreasing an implantation voltage potential between the ion plasma and the substrate, ions of the plasma accelerating towards and implanting <u>into a gate dielectric layer</u> formed on the substrate after an increase in magnitude of the implantation voltage potential; and
> forming a conductive transistor gate on the dielectric layer implanted with the ions. (Emphasis added)

A tool is described in the present patent application from page 5, line 3 to page 9, line 4, which is essentially the same as the tool described in Goeckner. The Examiner states that it would be obvious to use the tool described in Goeckner for the application as claimed, namely for modifying a gate dielectric layer of a transistor. An inventor has submitted an affidavit stating his reasons why one skilled in the art would not be inclined to use the tool in Goeckner to carry out the invention as claimed. Appellants argue that the Examiner has placed himself in the shoes of a person of ordinary skill in the art, which he is not, and that the

Examiner has not given sufficient weight to the affidavit of the inventor, who is a person of more than ordinary skill in the art. The inventor's affidavit is enclosed herewith as Appendix B.

IX. CONCLUSION

For the foregoing reasons, the Appellants respectfully assert that claim 1 overcomes the cited references and are therefore patentable. Independent claims 16 and 20 include similar limitations to the limitations of claim 1 that render claim 1 patentable. Those dependent claims not specifically addressed within one or more of the above claim Groups are deemed allowable in view of their dependency from an independent claim as argued above in addition to adding further limitations of their own. For the reasons presented herein, the removal of the present rejections and allowance of the present claims is respectfully requested.

If there are any further charges not accounted for herein, please charge them to our deposit account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Date: 1/12/04

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Reg. No. 46,503

12400 Wilshire Boulevard
Seventh Floor
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X. APPENDIX A

The claims on appeal read as follows:

1. (Original) A method of making a semiconductor transistor, comprising:

locating a substrate of a doped semiconductor material in a chamber;

introducing a gas into the chamber;

repeatedly increasing and decreasing a plasma generating voltage potential across the gas in the chamber between a cathode and an anode while the substrate is in the chamber, a transient ion plasma generating from the gas after an increase in magnitude of the plasma generating voltage potential and degenerating after a decrease in magnitude of the plasma generating voltage potential;

repeatedly increasing and decreasing an implantation voltage potential between the ion plasma and the substrate, ions of the plasma accelerating towards and implanting into a gate dielectric layer formed on the substrate after an increase in magnitude of the implantation voltage potential; and

forming a conductive transistor gate on the dielectric layer implanted with the ions.

2. (Original) The method of claim 1 wherein the gas includes nitrogen.

3. (Original) The method of claim 2 wherein the ions include nitrogen ions.

4. (Original) The method of claim 1 wherein the plasma generating voltage is generated by repeatedly increasing a voltage of the cathode to a positive voltage

and decreasing the voltage of the cathode.

5. (Original) The method of claim 1 wherein the plasma generating voltage has a magnitude of at least 1 kV.

6. (Original) The method of claim 1 wherein subsequent increases in the plasma generating voltage are spaced by less than 1 second.

7. (Original) The method of claim 1 wherein the plasma generating voltage is less than 50% of its maximum for at least 95% of the time.

8. (Original) The method of claim 1 wherein the ion plasma generates in an area in the chamber between the anode and the substrate.

9. (Original) The method of claim 1 wherein the implantation voltage potential has a maximum voltage potential that has a maximum magnitude of less than 80 V.

10. (Original) The method of claim 9 wherein the implantation voltage potential has a maximum magnitude of more than 10V.

11. (Original) The method of claim 1 wherein the implantation voltage potential has a magnitude of less than 4% of a maximum magnitude of the plasma generating voltage.

12. (Original) The method of claim 1 wherein a period of the implantation voltage potential is substantially the same as a period of the plasma generating voltage potential.

13. (Original) The method of claim 1 wherein the plasma generating voltage potential is generated by applying a voltage having a positive maximum to the cathode and the implantation voltage potential is created by applying a voltage having a negative maximum to the substrate.

14. (Original) The method of claim 1 wherein the ions increase a dielectric constant of the gate dielectric layer.

15. (Original) The method of claim 1 further comprising:

adjusting a magnitude of the implantation voltage potential.

16. (Original) A method of making a semiconductor transistor, comprising:

locating a substrate of a doped semiconductor material in a chamber;

introducing a gas into the chamber;

repeatedly increasing a voltage on a cathode to a positive value and decreasing the voltage on the cathode so as to repeatedly increase and decrease a plasma generating voltage potential across the gas in the chamber between the cathode and an anode while the substrate is in the chamber, an ion plasma generating from the gas after an increase in magnitude of the plasma

generating voltage potential and degenerating after a decrease in magnitude of the plasma generating voltage potential;

repeatedly decreasing a voltage on the substrate to a negative value and increasing the voltage on the substrate so as to repeatedly decrease and increase an implantation voltage potential between the ion plasma and the substrate, ions of the plasma accelerating towards and implanting into a gate dielectric layer formed on the substrate after a decrease of the implantation voltage potential; and

forming a conductive transistor gate on the dielectric layer implanted with the ions.

17. (Original) The method of claim 16 wherein the implantation voltage potential has a maximum magnitude of more than 10V but less than 20V.

18. (Original) The method of claim 16 wherein a period of the implantation voltage potential is substantially the same as a period of the plasma generating voltage potential.

19. (Original) The method of claim 16 wherein the ions increase a dielectric constant of the gate dielectric layer.

20. (Original) A method of making a semiconductor transistor, comprising:

locating a substrate of a doped semiconductor material in a chamber;

introducing a gas into the chamber;

repeatedly

(i) (a) increasing a plasma generating voltage potential across the gas in the chamber between a cathode and an anode while the substrate is in the chamber, a transient ion plasma generating from the gas after an increase in magnitude of the plasma generating voltage potential, and (b) decreasing an implantation voltage potential between the ion plasma and the substrate, the ions accelerating towards and implanting into a gate dielectric layer formed on the substrate after an increase in magnitude of the implantation voltage potential and

(ii) (a) decreasing the plasma generating voltage potential, the plasma degenerating after a decrease in magnitude of the plasma generating voltage potential, and (b) increasing the implantation voltage potential, whereafter fewer ions implant into the gate dielectric layer; and

forming a conductive transistor gate on the dielectric layer implanted with the ions.

21. (Original) The method of claim 20 wherein subsequent increases in the plasma generating voltage are spaced by less than 1 second.

22. (Original) The method of claim 20 wherein the plasma generating voltage is less than 50% of its maximum for at least 95% of the time.

IX. APPENDIX B

Attorney's Docket No.: 042390P10625 Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)
	)
Jack Hwang, et al.	)
	) Examiner: Igwe U. Anya
Application No.: 09/887,910	)
	) Art Unit: 2825
Filed: June 22, 2001	)
	)
For: A METHOD OF MAKING A SEMICONDUCTOR TRANSISTOR BY IMPLANTING IONS INTO A GATE DIELECTRIC LAYER THEREOF	)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AFFIDAVIT

Dear Sir:

I, Jack Hwang, having personal knowledge of the facts set forth herein, hereby declare as follows:

1. I am a co-inventor for the above-identified patent application entitled "A METHOD OF MAKING A SEMICONDUCTOR TRANSISTOR BY IMPLANTING IONS INTO A GATE DIELECTRIC LAYER THEREOF."

2. The Examiner has rejected claims 1-12, 14, 15 and 20-22 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,335,536 issued to Goeckner et al. ("Goeckner") in view of U.S. Patent No. 6,087,229 issued to Aronowitz et al. ("Aronowitz").

The Examiner has rejected claims 13, and 16-19 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,335,536 issued to Goeckner et al. ("Goeckner") in view of U.S. Patent No. 6,087,229 issued to Aronowitz et al. ("Aronowitz"), and further in view of U.S. Patent No. 6,432,780 issued to Chen.

3. The Goeckner patent appears to have been assigned to Varian Semiconductor Associates, hereinafter "Varian." The Goeckner patent discloses a tool that is provided by Varian, hereinafter "the Varian tool."

4. Varian is an ion implantation company, and the Varian tool is a gate electrode plasma tool which is an alternative to an ion plantation tool used for implanting conductivity-altering impurities into semiconductor wafers. The Varian tool is typically used to implant ions to form source and drain regions of transistors.

5. We use the Varian tool, which we have modified to provide one order of magnitude less power. The application is also different in that our tool is used for implanting ions into a gate dielectric layer of a transistor, as claimed.

6. The Varian field of ion implantation is worlds apart from the present application of gate dielectric formation. The people of Varian are skilled in the field of ion implantation, but are generally much less skilled in the field of gate dielectric formation. I have a background in ion implantation and was then transferred within my company to a group that specializes in the formation of gate dielectric layers. I believe that the only reason why the Varian tool found application in the formation of gate dielectric layers is because I was transferred,

and was able to apply the knowledge gained in this prior ion implantation field to the formation of gate dielectric layers.

7. I approached Varian and told Varian about the possible new application for the Varian tool by modifying the tool. The people of Varian were quite surprised to learn that the energy levels of their machine can be reduced by one order of magnitude and still find a new application.

8. I believe that a person, such as employed by Varian, having skill in the art and having knowledge of the prior art, would not have been able to modify the prior art to render the present invention. As such, I believe that the invention as claimed is patentable over the Varian tool.

I hereby declare that all statements made herein are of my own personal knowledge and are true, and that all statements made on information and belief are believed to be true; and that these statements were made with knowledge that willful, false statements and the like may jeopardize the validity of the patent application, or any patent resulting therefrom.

Respectfully submitted,

Dated: October 6, 2003

Jack Hwang

Jack Hwang

OIPE JAN 15 2004 PATENT & TRADEMARK OFFICE

Attorney's Docket No. 042390P10625 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In Re Application of:

Jack Hwang, et al.

Application No.: 09/887,910

Filed: June 22, 2001

For: A METHOD OF MAKING A SEMICONDUCTOR TRANSISTOR BY IMPLANTING IONS INTO A GATE DIELECTRIC LAYER THEREOF

Examiner: Igwe U. Anya

Art Unit: 2825

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P.O. Box 1450
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APPEAL BRIEF
IN SUPPORT OF APPELLANTS' APPEAL
TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Dear Sir:

The Appellants hereby submit this Brief in triplicate in support of their appeal from a final decision by the Examiner, mailed November 5, 2003, in the above-captioned case. The Appellants respectfully request consideration of this appeal by the Board of Patent Appeals and Interferences for allowance of the above-captioned patent application.

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Date of Deposit

Valerie J. Sterling
Name of Person Mailing Correspondence

Valerie J. Sterling
Signature

1-12-04
Date

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I. REAL PARTY IN INTEREST

The real party in interest is Intel Corporation, a corporation of Delaware having a principle place of business at 2200 Mission College Blvd., Santa Clara, CA 95052.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

III. STATUS OF THE CLAIMS

Claims 1-22 are currently pending. Claims 1-22 currently stand rejected by the Examiner under the Final Rejection mailed August 20, 2003. Claims 1-12, 14, 15 and 20-22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Goeckner et al., US Patent Number 6,335,536 (hereinafter Goeckner) in view of Aronowitz et al., US Patent Number 6,087,229 (hereinafter Aronowitz). Claims 13 and 16-19 stand rejected as being unpatentable over Goeckner in view of Aronowitz and further in view of Chen, US Patent Number 6,432,780 (hereinafter Chen).

IV. STATUS OF AMENDMENTS

A copy of all claims on appeal is attached in Appendix A hereto.

V. SUMMARY OF THE INVENTION

The present invention describes and claims a method of making a semiconductor transistor. A wafer substrate is inserted through the slit into the

chamber and located on the upper surface of a stand. The wafer substrate is at substantially the same voltage as the stand. (Page 9, lines 5-7)

Nitrogen gas is introduced through an inlet port into the chamber and flows into a cylindrical cathode. A constant flow of nitrogen gas flows into the inlet port and out of the outlet port. (Page 9, lines 8-10)

When a voltage is created on the cylindrical cathode, a voltage difference between the cylindrical cathode and the chamber increases. The increase in the voltage difference generates a transient ion plasma out of some of the nitrogen gas. The ion plasma consists of nitrogen ions having positive charge. The plasma is located within the cylindrical cathode above the substrate. An upper edge of the plasma is located near an upper wall of the chamber. A lower edge of the plasma is located distant from an upper surface of the wafer substrate so that a gap exists between the lower edge of the plasma and an upper surface of the wafer substrate. The gap is a few millimeters wide. (Page 9, lines 11-20)

The wafer substrate is made of a doped semiconductor material such as P-doped silicon. A thin gate dielectric layer is formed on the wafer substrate prior to its insertion into the chamber. The gate dielectric layer forms part of a transistor which is subsequently manufactured in and on the wafer substrate. For optimal performance of the transistor, it is required that the gate dielectric layer be very thin and be made of a material with a high k-value. The gate dielectric layer, when inserted into the chamber, is typically made of silicon dioxide having a thickness of approximately 20Å. The silicon dioxide gate dielectric layer is formed by exposing the silicon wafer substrate to oxygen in water. (Page 9, line 21 to Page 10, line 9)

A disadvantage of a silicon dioxide gate dielectric layer is that it has a relatively low k-value of about 3.9. A silicon nitride gate dielectric layer by contrast has a relatively high k-value of about 7.5, which is more desirable. The k-value of a silicon dioxide gate dielectric layer can be increased by implanting nitrogen molecules into the silicon dioxide gate dielectric layer. (Page 10, lines 10-14)

An ion plasma concentration increases when a voltage is applied to the circular cathode. The voltage on the cathode 38 is switched off before the plasma can reach a steady-state condition. The plasma, when existing, is thus in a transient condition at all times. By maintaining the plasma in a transient state the ion energy can be controlled. (Page 10, lines 15-20)

By pulsing the voltage on the stand, a voltage differential of -10 V is created between the stand and the plasma. The voltage potential only exists when an implanting switch is closed. Ions of the plasma are accelerated from the plasma towards the silicon dioxide gate dielectric layer when the implanting switch is closed. When an implanting switch is open, the ions are not accelerated towards the gate dielectric layer. (Page 10, line 21 to Page 11, line 6)

The combined effect of the creation of the confined transient plasma utilizing the plasma generating apparatus and creating a pulsed voltage on the stand, results in tight control in the amount and the energy of ions being implanted into the gate dielectric layer. The energy of the ions being implanted can be sharply defined and controlled for an optimum profile. (Page 11, lines 7-11)

A result of the implantation is that a k-value of the gate dielectric layer is increased while the composition of the silicon of the wafer substrate directly below the silicon dioxide layer remains unchanged. (Page 11, lines 16-19)

The wafer substrate is subsequently removed from the chamber and a multitude of semiconductor devices, including transistors, are formed thereon. A conductive gate is formed directly on the gate dielectric layer. N-doped source and drain regions are formed on opposing sides of the gate. Subsequent metalization and dielectric layers are formed above the transistor. A supply voltage can be provided through one metal line to the source and a drain voltage can be connected to a metal line connected to the drain. When a voltage is applied to the gate, current flows from the source to the drain. The current from the source to the drain is thus switched by applying a voltage to the gate. A switch speed of the current is increased because the gate dielectric layer is relatively thin and its k-value is relatively high. The current from the source to the drain is however not affected by any impurities. (Page 12, lines 3-16)

VI. ISSUES

The issues presented in this appeal are whether claims 1-20 are unpatentable under:

- 35 U.S.C. § 103 as being obvious over Goeckner in view of Aronowitz;

  and

- U.S.C. § 103 as being obvious over Goeckner in view of Aronowitz and further in view of Chen.

VII. GROUPING OF CLAIMS

For the purpose of this appeal, all the claims stand or fall together.

VIII. ARGUMENT; REJECTION OF THE PRESENT INVENTION IS IMPROPER SINCE ONE SKILLED IN THE ART WITH KNOWLEDGE OF THE PRIOR ART WOULD NOT HAVE USED THE PRIOR ART TO COME UP WITH THE INVENTION AS CLAIMED

Claim 1 recites:

> 1. A method of making a semiconductor transistor, comprising:
> locating a substrate of a doped semiconductor material in a chamber;
> introducing a gas into the chamber;
> repeatedly increasing and decreasing a plasma generating voltage potential across the gas in the chamber between a cathode and an anode while the substrate is in the chamber, a transient ion plasma generating from the gas after an increase in magnitude of the plasma generating voltage potential and degenerating after a decrease in magnitude of the plasma generating voltage potential;
> repeatedly increasing and decreasing an implantation voltage potential between the ion plasma and the substrate, ions of the plasma accelerating towards and implanting <u>into a gate dielectric layer</u> formed on the substrate after an increase in magnitude of the implantation voltage potential; and
> forming a conductive transistor gate on the dielectric layer implanted with the ions. (Emphasis added)

A tool is described in the present patent application from page 5, line 3 to page 9, line 4, which is essentially the same as the tool described in Goeckner. The Examiner states that it would be obvious to use the tool described in Goeckner for the application as claimed, namely for modifying a gate dielectric layer of a transistor. An inventor has submitted an affidavit stating his reasons why one skilled in the art would not be inclined to use the tool in Goeckner to carry out the invention as claimed. Appellants argue that the Examiner has placed himself in the shoes of a person of ordinary skill in the art, which he is not, and that the

Examiner has not given sufficient weight to the affidavit of the inventor, who is a person of more than ordinary skill in the art. The inventor's affidavit is enclosed herewith as Appendix B.

IX. CONCLUSION

For the foregoing reasons, the Appellants respectfully assert that claim 1 overcomes the cited references and are therefore patentable. Independent claims 16 and 20 include similar limitations to the limitations of claim 1 that render claim 1 patentable. Those dependent claims not specifically addressed within one or more of the above claim Groups are deemed allowable in view of their dependency from an independent claim as argued above in addition to adding further limitations of their own. For the reasons presented herein, the removal of the present rejections and allowance of the present claims is respectfully requested.

If there are any further charges not accounted for herein, please charge them to our deposit account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Date: 1/12/04

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X. APPENDIX A

The claims on appeal read as follows:

1. (Original) A method of making a semiconductor transistor, comprising:

locating a substrate of a doped semiconductor material in a chamber;

introducing a gas into the chamber;

repeatedly increasing and decreasing a plasma generating voltage potential across the gas in the chamber between a cathode and an anode while the substrate is in the chamber, a transient ion plasma generating from the gas after an increase in magnitude of the plasma generating voltage potential and degenerating after a decrease in magnitude of the plasma generating voltage potential;

repeatedly increasing and decreasing an implantation voltage potential between the ion plasma and the substrate, ions of the plasma accelerating towards and implanting into a gate dielectric layer formed on the substrate after an increase in magnitude of the implantation voltage potential; and

forming a conductive transistor gate on the dielectric layer implanted with the ions.

2. (Original) The method of claim 1 wherein the gas includes nitrogen.

3. (Original) The method of claim 2 wherein the ions include nitrogen ions.

4. (Original) The method of claim 1 wherein the plasma generating voltage is generated by repeatedly increasing a voltage of the cathode to a positive voltage

and decreasing the voltage of the cathode.

5. (Original) The method of claim 1 wherein the plasma generating voltage has a magnitude of at least 1 kV.

6. (Original) The method of claim 1 wherein subsequent increases in the plasma generating voltage are spaced by less than 1 second.

7. (Original) The method of claim 1 wherein the plasma generating voltage is less than 50% of its maximum for at least 95% of the time.

8. (Original) The method of claim 1 wherein the ion plasma generates in an area in the chamber between the anode and the substrate.

9. (Original) The method of claim 1 wherein the implantation voltage potential has a maximum voltage potential that has a maximum magnitude of less than 80 V.

10. (Original) The method of claim 9 wherein the implantation voltage potential has a maximum magnitude of more than 10V.

11. (Original) The method of claim 1 wherein the implantation voltage potential has a magnitude of less than 4% of a maximum magnitude of the plasma generating voltage.

12. (Original) The method of claim 1 wherein a period of the implantation voltage potential is substantially the same as a period of the plasma generating voltage potential.

13. (Original) The method of claim 1 wherein the plasma generating voltage potential is generated by applying a voltage having a positive maximum to the cathode and the implantation voltage potential is created by applying a voltage having a negative maximum to the substrate.

14. (Original) The method of claim 1 wherein the ions increase a dielectric constant of the gate dielectric layer.

15. (Original) The method of claim 1 further comprising:

adjusting a magnitude of the implantation voltage potential.

16. (Original) A method of making a semiconductor transistor, comprising:

locating a substrate of a doped semiconductor material in a chamber;

introducing a gas into the chamber;

repeatedly increasing a voltage on a cathode to a positive value and decreasing the voltage on the cathode so as to repeatedly increase and decrease a plasma generating voltage potential across the gas in the chamber between the cathode and an anode while the substrate is in the chamber, an ion plasma generating from the gas after an increase in magnitude of the plasma

generating voltage potential and degenerating after a decrease in magnitude of the plasma generating voltage potential;

repeatedly decreasing a voltage on the substrate to a negative value and increasing the voltage on the substrate so as to repeatedly decrease and increase an implantation voltage potential between the ion plasma and the substrate, ions of the plasma accelerating towards and implanting into a gate dielectric layer formed on the substrate after a decrease of the implantation voltage potential; and

forming a conductive transistor gate on the dielectric layer implanted with the ions.

17. (Original) The method of claim 16 wherein the implantation voltage potential has a maximum magnitude of more than 10V but less than 20V.

18. (Original) The method of claim 16 wherein a period of the implantation voltage potential is substantially the same as a period of the plasma generating voltage potential.

19. (Original) The method of claim 16 wherein the ions increase a dielectric constant of the gate dielectric layer.

20. (Original) A method of making a semiconductor transistor, comprising:

locating a substrate of a doped semiconductor material in a chamber;

introducing a gas into the chamber;

repeatedly

(i) (a) increasing a plasma generating voltage potential across the gas in the chamber between a cathode and an anode while the substrate is in the chamber, a transient ion plasma generating from the gas after an increase in magnitude of the plasma generating voltage potential, and (b) decreasing an implantation voltage potential between the ion plasma and the substrate, the ions accelerating towards and implanting into a gate dielectric layer formed on the substrate after an increase in magnitude of the implantation voltage potential and

(ii) (a) decreasing the plasma generating voltage potential, the plasma degenerating after a decrease in magnitude of the plasma generating voltage potential, and (b) increasing the implantation voltage potential, whereafter fewer ions implant into the gate dielectric layer; and

forming a conductive transistor gate on the dielectric layer implanted with the ions.

21. (Original) The method of claim 20 wherein subsequent increases in the plasma generating voltage are spaced by less than 1 second.

22. (Original) The method of claim 20 wherein the plasma generating voltage is less than 50% of its maximum for at least 95% of the time.

IX. APPENDIX B

Attorney's Docket No.: 042390P10625 Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Jack Hwang, et al. Application No.: 09/887,910 Filed: June 22, 2001 For: A METHOD OF MAKING A SEMICONDUCTOR TRANSISTOR BY IMPLANTING IONS INTO A GATE DIELECTRIC LAYER THEREOF	Examiner: Igwe U. Anya Art Unit: 2825

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AFFIDAVIT

Dear Sir:

I, Jack Hwang, having personal knowledge of the facts set forth herein, hereby declare as follows:

1. I am a co-inventor for the above-identified patent application entitled "A METHOD OF MAKING A SEMICONDUCTOR TRANSISTOR BY IMPLANTING IONS INTO A GATE DIELECTRIC LAYER THEREOF."

2. The Examiner has rejected claims 1-12, 14, 15 and 20-22 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,335,536 issued to Goeckner et al. ("Goeckner") in view of U.S. Patent No. 6,087,229 issued to Aronowitz et al. ("Aronowitz").

The Examiner has rejected claims 13, and 16-19 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,335,536 issued to Goeckner et al. ("Goeckner") in view of U.S. Patent No. 6,087,229 issued to Aronowitz et al. ("Aronowitz"), and further in view of U.S. Patent No. 6,432,780 issued to Chen.

3. The Goeckner patent appears to have been assigned to Varian Semiconductor Associates, hereinafter "Varian." The Goeckner patent discloses a tool that is provided by Varian, hereinafter "the Varian tool."

4. Varian is an ion implantation company, and the Varian tool is a gate electrode plasma tool which is an alternative to an ion plantation tool used for implanting conductivity-altering impurities into semiconductor wafers. The Varian tool is typically used to implant ions to form source and drain regions of transistors.

5. We use the Varian tool, which we have modified to provide one order of magnitude less power. The application is also different in that our tool is used for implanting ions into a gate dielectric layer of a transistor, as claimed.

6. The Varian field of ion implantation is worlds apart from the present application of gate dielectric formation. The people of Varian are skilled in the field of ion implantation, but are generally much less skilled in the field of gate dielectric formation. I have a background in ion implantation and was then transferred within my company to a group that specializes in the formation of gate dielectric layers. I believe that the only reason why the Varian tool found application in the formation of gate dielectric layers is because I was transferred,

and was able to apply the knowledge gained in this prior ion implantation field to the formation of gate dielectric layers.

7. I approached Varian and told Varian about the possible new application for the Varian tool by modifying the tool. The people of Varian were quite surprised to learn that the energy levels of their machine can be reduced by one order of magnitude and still find a new application.

8. I believe that a person, such as employed by Varian, having skill in the art and having knowledge of the prior art, would not have been able to modify the prior art to render the present invention. As such, I believe that the invention as claimed is patentable over the Varian tool.

I hereby declare that all statements made herein are of my own personal knowledge and are true, and that all statements made on information and belief are believed to be true; and that these statements were made with knowledge that willful, false statements and the like may jeopardize the validity of the patent application, or any patent resulting therefrom.

Respectfully submitted,

Dated: October 6, 2003

Jack Hwang

image

AF/2825 $

FEE TRANSMITTAL FOR FY 2004

(FY 2004 Begins 10/01/2003)

TOTAL AMOUNT OF PAYMENT ($) 330.00

Complet if Known:

Application No. 09/887,910
Filing Dat June 22, 2001
First Nam d Inventor Jack Hwang
Examiner Name Igwe U. Anya
Art Unit 2825
Attorney Docket No. 042390P10625

____ **Applicant claims small entity status. See 37 CFR 1.27.**

METHOD OF PAYMENT (check all that apply)

X Check ____ Credit Card ____ Money Order ____ Other ____ None

X Deposit Account
Deposit Account Number : 02-2666
Deposit Account Name: ____

X The Director is Authorized to do the following with respect to the above-identified Deposit Account:
- ____ **Charge fee(s) indicated below.**
- **X Credit any overpayments.**
- **X Charge any additional fees during the pendency of this application.**
- **X Any concurrent or future reply that requires a petition for extension of time should be treated as incorporating an appropriate petition for extension of time and all required fees should be charged.**
- ____ **Charge fee(s) indicated below except for the filing fee.**

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility application filing fee	
1002	340	2002	170	Design application filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional application filing fee	

SUBTOTAL (1) $ 0.00

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

			Extra Claims		Fee from below		Fee Paid
Total Claims	____	– 20** =	____	X	____	=	____
Independent Claims	____	– 3** =	____	X	____	=	____
Multiple Dependent					____	=	____

****Or number previously paid, if greater; For Reissues, see below.**

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dep nd nt claim, if n t paid
1204	86	2204	43	**R issue ind pendent claims over riginal patent
1205	18	2205	9	**R issue claims in excess of 20 and v r original patent

SUBTOTAL (2) $ 0.00

Based on Form PTO/SB/17 (08-03) as modified by BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP on 09/30/03.

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Larg Entity F e Cod	Fee ($)	Small Entity F C de	Fe ($)	F Description	F e Paid
1051	130	2051	65	Surcharg - late filing f e r oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for ex parte reexamination	
1813	8,800	1813	8,800	Request for inter parties reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	330.00
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive – unavoidable	
1453	1,330	2453	665	Petition to revive - unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	For filing a submission after final rejection (see 37 CFR 1.129(a))	
1814	110	2814	55	Statutory Disclaimer	
1810	770	2810	385	For each additional invention to be examined (see 37 CFR 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	
1504	300	1504	300	Publication fee for early, voluntary, or normal pub.	
1505	300	1505	300	Publication fee for republication	
1803	130	1803	130	Request for voluntary publication or republication	
1808	130	1808	130	Processing fee under 37 CFR 1.17(i) (except provisionals)	
1454	1,330	1454	1,330	Acceptance of unintentionally delayed claim for priority	

Other fee (specify) ____________________ ______

Other fee (specify) ____________________ ______

SUBTOTAL (3) $ 330.00

*Reduced by Basic Filing Fee Paid

SUBMITTED BY:

Typed or Printed Name: Stephen M. De Klerk

Signature: [signature] Date: 1/12/04

Reg. Number: 46,503 Telephone Number: (408) 720-8300

Send to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450